IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of

Yuji MURAYAMA et al.

Art Unit: **2876**

Serial No. **09/739,318**

Examiner: E. Labaze

Filed: December 19, 2000

For: PORTABLE ELECTRONIC APPARATUS, IC CARD AND READER/WRITER

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Three copies of an Appellant's Brief on Appeal for the above-referenced application are being filed herewith. Thus, consideration of the Appeal Brief is respectfully requested.

A Notice of Appeal and fee was filed on March 4, 2003, and an Appeal Brief and fee was filed May 5, 2003. Thus, it is believed that **no fees are due**. M.P.E.P. §1208.02. However, if a fee is required, the Commissioner is hereby authorized to charge the fee to Deposit Account # 18-0013.

Respectfully submitted,

DATE: October 2., 2003

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Sir:

This is an Appeal Brief under Rule 192 appealing the decision of the Examiner dated August 5, 2003 (Paper No. 18). Each of the topics required by Rule 192 is presented herewith and is labeled appropriately.

I. Real Party In Interest

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the

inventor and recorded by the U.S. Patent and Trademark Office at **reel 011865, frame 0206.**

II. Related Appeals And Interferences

There are no appeals or interferences related to the present application of which Appellant is aware.

III. Status of Claims

Claims 1-12 were originally filed and are pending in this application.

The Request for Reconsideration of September 24, 2002 canceled claims 1-12 and added claims 13-37.

Accordingly, appellant hereby appeals the rejection of pending claims 13-37, which are presented in the Appendix.

IV. Status of Amendments

There are no amendments filed subsequent to the Office Action of August 5, 2003.

V. Summary of the Invention

The present invention relates to a portable electronic apparatus, an IC card and a reader/writer.

Described within figures 1-5 is a clock generation circuit 25. The clock generation circuit 25 uses a received signal S2,S3 to generate a clock signal CK and a sampling signal P8, wherein received data is the information transmitted to the portable electronic apparatus by way of the received signal S2,S3.

A decoder decodes a plurality of logic levels to generate the received data. As shown within figure 2, the sampling signal P8 has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels are generated during each cycle of clock signal. A logic level DS of the plurality of logic levels is the signal level of the received signal S2,3 when sampled by a pulse of the plurality of pulses.

Described within figures 6-10 is a clock generation circuit 25 that uses a received signal S2,S3 to generate a clock signal CK, wherein the received data D2,3 is the information transmitted to by way of the received signal S2,S3.

A correlation value detection circuit 32 compares the phase of the clock signal CK to the phase of the received signal S2,S3 to generate a correlation value signal. As shown within figures 7-9, the correlation value signal trends in a first direction when the clock signal CK is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal CK is out of phase with the received signal S2,S3.

A determination circuit 33 uses the correlation value signal to generate the received data.

VI. Issues

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in rejecting claims 13-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,161,762 to Bashan et al. (Bashan).

Whether the Examiner erred in rejecting claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Bashan in

view of U.S. Patent No. 5,574,754 to Kurihara et al. (Kurihara).

These issues will be discussed hereinbelow.

VII. Grouping of Claims

For purposes of the issues presented by this appeal:

Claim 13, 16, 17 stand or fall together.

Claim 14 stands or falls separately.

Claim 15 stands or falls separately.

Claim 18, 21 stand or fall together.

Claim 19 stands or falls separately.

Claim 20 stands or falls separately.

Claim 22, 25 stand or fall together.

Claim 23 stands or falls separately.

Claim 24 stands or falls separately.

Claim 26 stands or falls separately.

Claim 27 stands or falls separately.

Claim 28 stands or falls separately.

Claim 29 stands or falls separately.

Claim 30 stands or falls separately.

Claim 31 stands or falls separately.

Claim 33 stands or falls separately.

Claim 32 stands or falls separately.

Claim 34 stands or falls separately.

Claim 35 stands or falls separately.

Claim 36 stands or falls separately.

Claim 37 stands or falls separately.

The arguments set forth in the following section provide reasons why these groups are considered patentable, 37 C.F.R. §1.192 (c)(7).

VIII. Arguments

In the Office Action of August 5, 2003:

The Examiner rejected claims 13-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,161,762 to Bashan et al. (Bashan).

The Examiner rejected claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Bashan in view of U.S. Patent No. 5,574,754 to Kurihara et al. (Kurihara).

For at least the following reasons, Appellant submits that these rejections are both technically and legally unsound and should therefore be reversed.

Reopened prosecution

This Appeal Brief has been submitted in response to the rejection of the Examiner made within the non-final Office Action of August 5, 2003 that *reopened prosecution* of the above-identified application following the filing on May 5, 2003 of the previous Appeal Brief.

General Matters

M.P.E.P. 707.07(f) states that "the importance of answering such arguments is illustrated by In re Herrmann, 261 F.2d 598, 120 USPQ 182 (CCPA 1958) where the applicant urged that the subject matter claimed produced new and useful results. The court noted that since applicant's statement of advantages was not questioned by the examiner or the Board of Appeals, it was constrained to accept the statement at face value and therefore found certain claims to be allowable. See also In re Soni, 54 F.3d 746, 751, 34 USPQ2d 1684, 1688 (Fed Cir. 1995) (Office failed to rebut applicant's argument)."

The Examiner erred in rejecting claims 13-25 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 6,161,762 to Bashan et al. (Bashan).

This rejection is respectfully traversed, at least for the following reasons.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

These features are depicted at least within figures 1 and 5 of the specification as originally filed. Nevertheless, these features are not found within Bashan.

As described within the specification for the above-identified application, independent claims 13, 18 and 22, and the claims dependent thereon, include a clock generation circuit 25 using a received signal S2,3 to generate a clock signal CK and a sampling signal P8 (figure 1). Received data D2,3 are the

information transmitted to the portable electronic apparatus by way of the received signal S2,3. The sampling signal P8 has a plurality of pulses P8 present during each cycle of the clock signal CK (figure 5). A plurality of logic levels is generated during each cycle of the clock signal (figure 5). A logic level of the plurality of logic levels is the signal level of the received signal S2,3 when sampled by a pulse P8 of the plurality of pulses P8 (figure 2). A decoder 28 decodes the plurality of logic levels P8 to generate the received data D2,3 (figures 1 and 3).

Claim 13, 16, 17

Claim 13 and the claims dependent thereon are drawn to a portable electronic apparatus comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to the portable electronic apparatus by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

Within claim 13, the clock generation circuit uses a received signal to generate a clock signal and a sampling signal. The sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal, and a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses. These features are not found within Bashan, either explicitly or implicitly.

Figure 1B of Bashan arguably depicts L1 and L2 as inputs to clock generator 51. The clock generator 51 (figure 1B) arguably creates different clock signals according to whether the data transaction system 10 is in contact or contactless mode (column 13, lines 56-58). Specifically, if in contact mode, the clock 51 is tristate so as to allow the desired clock signal CLK to be fed externally to the microprocessor 14 via the contact "CLK" in the contact field 11 (figure 1A, column 13, lines 58-61). In contactless mode, there is fed to the microprocessor 14 a clock signal whose frequency is an integer division of the transmitted carrier signal, the division ratio being variable and set by respective E^2 bits in the EEPROM 53 (column 13, lines 61-65).

Nevertheless, Bashan fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a sampling signal, wherein the sampling signal has a plurality of pulses during each cycle of the clock signal. In this regard, a sampling signal having a plurality of pulses during each cycle of the clock signal is not found within Bashan.

The Office Action contend that the sampling signal is found within figures 8B-D and figures 9B-C. However, a review of these figures and the teaching found within Bashan fail to teach

figures 8B-D and figures 9B-C as depicting a sampling signal.

In particular, Bashan arguably teaches a contact/contactless smart card having customizable antenna interface.

Figure 1C of Bashan arguably depicts a "Low M" demodulator 48, which is shown within figure 8A. Figure 1C of Bashan arguably depicts a variable/loading means 45 having a "Low M" signal as an output (column 7, lines 41-43). Figure 8A shows schematically a demodulator for demodulating a "LOW M" modulated signal. Figures 8B, 8C and 8D show, respectively, the input data signal, the differentiated signal fed to the non-inverting input of the OP AMP 105 and the data signal appearing at the output of the comparator (column 12, line 66 to column 13, line 2). Figures 8B, 8C and 8D of Bashan fail to disclose, teach or suggest the output of the comparator as being the claimed sampling signal.

Figure 1C of Bashan arguably depicts a "High M" demodulator 49, which is shown within figure 9A. Figure 1C of Bashan arguably depicts modulated carrier signal L1 appearing at connector terminal 20, while figure 9B of Bashan arguably depicts a voltage V_{L1} for modulated carrier signal L1 and figure 9C

arguably depicts signal V_{OUT} appearing at the output of the comparator 110 of figure 9A (column 13, lines 9-11). Thus, figures 9A-C arguably depict the demodulation of signal L1 found at connector terminal 20, which is not the claimed sampling signal.

Bashan also fails to disclose, teach or suggest a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses.

Bashan also fails to disclose, teach or suggest a decoding the plurality of logic levels to generate the received data.

Bashan fails to disclose, teach or suggest at least a logic level of the plurality of logic levels being the signal level of a received signal when sampled by a pulse.

Claim 14

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 13 and at least for the following reasons.

Within claim 14, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out of phase with the received signal, is brought into phase with the received signal.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51). However, the feature of the generated clock signal of the parent claim, when out of phase with the received signal, being brought into phase with the received signal is not found within Bashan.

Claim 15

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 13 and at least for the following reasons.

Within claim 15, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

However, Bashan fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within the parent claim.

Moreover, Bashan fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory.

Claim 18, 21

Claim 18 and the claims dependent thereon are drawn to an IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, the IC card comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to the IC card by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

Within claim 18, the clock generation circuit uses a received signal to generate a clock signal and a sampling signal. The sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal, and a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses. These features are not found within Bashan, either explicitly or implicitly.

Figure 1B of Bashan arguably depicts L1 and L2 as inputs to clock generator 51. The clock generator 51 (figure 1B) arguably

creates different clock signals according to whether the data transaction system 10 is in contact or contactless mode (column 13, lines 56-58). Specifically, if in contact mode, the clock 51 is tristate so as to allow the desired clock signal CLK to be fed externally to the microprocessor 14 via the contact "CLK" in the contact field 11 (figure 1A, column 13, lines 58-61). In contactless mode, there is fed to the microprocessor 14 a clock signal whose frequency is an integer division of the transmitted carrier signal, the division ratio being variable and set by respective E^2 bits in the EEPROM 53 (column 13, lines 61-65).

Nevertheless, Bashan fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a sampling signal, wherein the sampling signal has a plurality of pulses during each cycle of the clock signal. In this regard, a sampling signal having a plurality of pulses during each cycle of the clock signal is not found within Bashan.

The Office Action contend that the sampling signal is found within figures 8B-D and figures 9B-C. However, a review of these figures and the teaching found within Bashan fail to teach figures 8B-D and figures 9B-C as depicting a sampling signal.

In particular, Bashan arguably teaches a contact/contactless smart card having customizable antenna interface.

Figure 1C of Bashan arguably depicts a "Low M" demodulator 48, which is shown within figure 8A. Figure 1C of Bashan arguably depicts a variable/loading means 45 having a "Low M" signal as an output (column 7, lines 41-43). Figure 8A shows schematically a demodulator for demodulating a "LOW M" modulated signal. Figures 8B, 8C and 8D show, respectively, the input data signal, the differentiated signal fed to the non-inverting input of the OP AMP 105 and the data signal appearing at the output of the comparator (column 12, line 66 to column 13, line 2). Figures 8B, 8C and 8D of Bashan fail to disclose, teach or suggest the output of the comparator as being the claimed sampling signal.

Figure 1C of Bashan arguably depicts a "High M" demodulator 49, which is shown within figure 9A. Figure 1C of Bashan arguably depicts modulated carrier signal L1 appearing at connector terminal 20, while figure 9B of Bashan arguably depicts a voltage V_{L1} for modulated carrier signal L1 and figure 9C arguably depicts signal V_{OUT} appearing at the output of the comparator 110 of figure 9A (column 13, lines 9-11). Thus,

figures 9A-C arguably depict the demodulation of signal L1 found at connector terminal 20, which is not the claimed sampling signal.

Bashan also fails to disclose, teach or suggest a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses.

Bashan also fails to disclose, teach or suggest a decoding the plurality of logic levels to generate the received data.

Bashan fails to disclose, teach or suggest at least a logic level of the plurality of logic levels being the signal level of a received signal when sampled by a pulse.

Claim 19

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 18 and at least for the following reasons.

Within claim 19, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out

of phase with the received signal, is brought into phase with the received signal.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51). However, the feature of the generated clock signal of the parent claim, when out of phase with the received signal, being brought into phase with the received signal is not found within Bashan.

Claim 20

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 18 and at least for the following reasons.

Within claim 20, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

However, Bashan fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within the parent claim.

Moreover, Bashan fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory.

Claim 22, 25

Claim 22 and the claims dependent thereon are drawn to a reader/writer for receiving data transmitted by an IC card, the reader/writer comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to the reader/writer by way of the received signal,

the sampling signal having a plurality of pulses during each cycle of the clock signal,

a plurality of logic levels being generated during the each cycle of the clock signal,

a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses; and

a decoder, the decoder decoding the plurality of logic levels to generate the received data.

Within claim 22, the clock generation circuit uses a received signal to generate a clock signal and a sampling signal. The sampling signal has a plurality of pulses during each cycle of the clock signal. A plurality of logic levels is generated during each cycle of the clock signal, and a logic level of the plurality of logic levels is the signal level of the received signal when sampled by a pulse of the plurality of pulses. These features are not found within Bashan, either explicitly or implicitly.

Figure 1B of Bashan arguably depicts L1 and L2 as inputs to clock generator 51. The clock generator 51 (figure 1B) arguably creates different clock signals according to whether the data

transaction system 10 is in contact or contactless mode (column 13, lines 56-58). Specifically, if in contact mode, the clock 51 is tristate so as to allow the desired clock signal CLK to be fed externally to the microprocessor 14 via the contact "CLK" in the contact field 11 (figure 1A, column 13, lines 58-61). In contactless mode, there is fed to the microprocessor 14 a clock signal whose frequency is an integer division of the transmitted carrier signal, the division ratio being variable and set by respective E^2 bits in the EEPROM 53 (column 13, lines 61-65).

Nevertheless, Bashan fails to disclose, teach or suggest a clock generation circuit that uses a received signal to generate a sampling signal, wherein the sampling signal has a plurality of pulses during each cycle of the clock signal. In this regard, a sampling signal having a plurality of pulses during each cycle of the clock signal is not found within Bashan.

The Office Action contend that the sampling signal is found within figures 8B-D and figures 9B-C. However, a review of these figures and the teaching found within Bashan fail to teach figures 8B-D and figures 9B-C as depicting a sampling signal.

In particular, Bashan arguably teaches a contact/contactless

smart card having customizable antenna interface.

Figure 1C of Bashan arguably depicts a "Low M" demodulator 48, which is shown within figure 8A. Figure 1C of Bashan arguably depicts a variable/loading means 45 having a "Low M" signal as an output (column 7, lines 41-43). Figure 8A shows schematically a demodulator for demodulating a "LOW M" modulated signal. Figures 8B, 8C and 8D show, respectively, the input data signal, the differentiated signal fed to the non-inverting input of the OP AMP 105 and the data signal appearing at the output of the comparator (column 12, line 66 to column 13, line 2). Figures 8B, 8C and 8D of Bashan fail to disclose, teach or suggest the output of the comparator as being the claimed sampling signal.

Figure 1C of Bashan arguably depicts a "High M" demodulator 49, which is shown within figure 9A. Figure 1C of Bashan arguably depicts modulated carrier signal L1 appearing at connector terminal 20, while figure 9B of Bashan arguably depicts a voltage V_{L1} for modulated carrier signal L1 and figure 9C arguably depicts signal V_{OUT} appearing at the output of the comparator 110 of figure 9A (column 13, lines 9-11). Thus, figures 9A-C arguably depict the demodulation of signal L1 found

at connector terminal 20, which is not the claimed sampling signal.

Bashan also fails to disclose, teach or suggest a logic level of the plurality of logic levels being the signal level of the received signal when sampled by a pulse of the plurality of pulses.

Bashan also fails to disclose, teach or suggest a decoding the plurality of logic levels to generate the received data.

Bashan fails to disclose, teach or suggest at least a logic level of the plurality of logic levels being the signal level of a received signal when sampled by a pulse.

Claim 23

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 22 and at least for the following reasons.

Within claim 23, the phase of the clock signal is compared to the phase of the received signal. The clock signal, when out

of phase with the received signal, is brought into phase with the received signal.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51). However, the feature of the generated clock signal of the parent claim, when out of phase with the received signal, being brought into phase with the received signal is not found within Bashan.

Claim 24

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 22 and at least for the following reasons.

Within claim 24, the decoder includes a storage medium. The plurality of logic levels is used to address a storage medium location within the storage medium. The received data is stored at the storage medium location.

However, Bashan fails to disclose, teach or suggest a ***plurality of logic levels*** being generated during the each cycle of the clock signal, as claimed within the parent claim.

Moreover, Bashan fails to disclose, teach or suggest the plurality of logic levels being used to address a storage medium location within memory.

The Examiner erred in rejecting claims 26-37 under 35 U.S.C. §103 as allegedly being obvious over Bashan in view of U.S. Patent No. 5,574,754 to Kurihara et al. (Kurihara).

This rejection is respectfully traversed, at least for the following reasons.

"The Patent and Trademark Office (PTO) has the burden of showing a prima facie case of obviousness." *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993). "In determining the propriety of the Patent Office case for prima facie obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification." *In re Taborsky*,

183 USPQ 50, 55 (CCPA 1974). Moreover, prima facie obviousness of a claimed invention is established "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

As described within the specification for the above-identified application, independent claims 26, 30 and 34, and the claims dependent thereon, include clock generation circuit 25 that uses a received signal S2,3 to generate a clock signal CK. Received data D2,3 are the information transmitted to the portable electronic apparatus by way of the received signal S2,3. A correlation value detection circuit 32 compares the phase of the clock signal CK to the phase of the received signal S2,3 to generate a correlation value signal K(x). The correlation value signal K(x) trends in a first direction when the clock signal CK is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal (figures 7-9). A determination circuit 33 uses the correlation value signal K(x) to generate the received data D2,3 (figure 6).

Claim 26

Claim 26 and the claims dependent thereon are drawn to a portable electronic apparatus comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the portable electronic apparatus by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 26, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51).

However, Bashan fails to disclose, teach or suggest a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with

the received signal.

Bashan also fails to disclose, teach or suggest a determination circuit that uses the correlation value signal to generate the received data.

The Office Action admits that Bashan fails to disclose, teach or suggest at least a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate received data, and cites Kurihara for the features admitted to be absent within Bashan.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate

a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received signal to generate a clock signal, as claimed.

Claim 27

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 27, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 28

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within the parent claim, the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. Within claim 28, the first direction is an increasing direction and the direction opposite to the first direction is a decreasing direction.

However, Bashan and Kurihara fail to disclose, teach or suggest the first direction is an increasing direction and the direction opposite to the first direction is a decreasing direction.

Claim 29

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 26, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 29, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 30

Claim 30 and the claims dependent thereon are drawn to an IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, the IC card comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the IC card by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 30, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. These

features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Bashan and Kurihara, either individually or as a whole.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51).

However, Bashan fails to disclose, teach or suggest a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal.

Bashan also fails to disclose, teach or suggest a determination circuit that uses the correlation value signal to generate the received data.

The Office Action admits that Bashan fails to disclose,

teach or suggest at least a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate received data, and cites Kurihara for the features admitted to be absent within Bashan.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received

signal to generate a clock signal, as claimed.

Claim 31

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 31, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 32

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 32, the first direction is an increasing direction and the direction opposite to the first direction is a

decreasing direction.

Claim 33

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 30 and at least for the following reasons.

Within claim 30, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 33, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 34

Claim 34 and the claims dependent thereon are drawn to an IC card, the reader/writer comprising:

a clock generation circuit, the clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to the reader/writer by way of the received signal; and

a correlation value detection circuit, the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal,

the correlation value signal trending in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal;

a determination circuit, the determination circuit using the correlation value signal to generate the received data.

Within claim 34, a received signal is used to generate a clock signal. In addition, the correlation value detection circuit compares the phase of the clock signal to the phase of

the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trends in a direction opposite to the first direction when the clock signal is out of phase with the received signal. These features are explained at least within figures 6 and 10 of the specification as originally filed. Yet, these features are not found within Bashan and Kurihara, either individually or as a whole.

Bashan arguably teaches that the reader may also detect the change in phase of the carrier signal relative to its own master clock so as to improve the accuracy with which data is read from the card (column 16, lines 47-51).

However, Bashan fails to disclose, teach or suggest a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal, wherein the correlation value signal trends in a first direction when the clock signal is in phase with the received signal and trending in a direction opposite to the first direction when the clock signal is out of phase with the received signal.

Bashan also fails to disclose, teach or suggest a determination circuit that uses the correlation value signal to generate the received data.

The Office Action admits that Bashan fails to disclose, teach or suggest at least a correlation value detection circuit that compares the phase of the clock signal to the phase of the received signal to generate received data, and cites Kurihara for the features admitted to be absent within Bashan.

While Kurihara arguably teaches a sliding correlator, Kurihara fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Instead, figures 2, 3 of Kurihara arguably depict input signal as a delayed input signal OUTPUT 1 and further depicts input signal as an non-delayed input signal OUTPUT 2 that are multiplied by multipliers 12, 13 and compared by comparator 16, but fails to disclose, teach or suggest a comparison of phase of the clock signal to the phase of the received signal to generate a correlation value signal, as claimed.

Figure 4 of Kurihara arguably depicts input signal as a digitized input signal from correlating unit 27 and further depicts a digitized input signal from correlating unit 28 (column 7, lines 48-49). While figure 4 depict clock generator 32, figure 4 fails to disclose, teach or suggest the use of a received signal to generate a clock signal, as claimed.

Claim 35

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 35, a value of the correlation value signal establishes the logic level of the received data, the logic level being one of a "0" logic level and a "1" logic level.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value detection circuit comparing the phase of the clock signal to the phase of the received signal to generate a correlation value signal.

Claim 36

The rejection of this claim respectfully traversed, at least

for reasons provided hereinabove regarding claim 26 and at least for the following reasons.

Within claim 34, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within claim 36, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Claim 37

The rejection of this claim respectfully traversed, at least for reasons provided hereinabove regarding claim 34 and at least for the following reasons.

Within claim 34, the correlation value detection circuit compares the phase of the clock signal to the phase of the received signal to generate a correlation value signal. Within

claim 37, the correlation value signal is bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

However, Bashan and Kurihara fail to disclose, teach or suggest the correlation value signal being bounded by a maximum amount and a minimum amount, the minimum amount being less than the maximum amount.

Conclusion

Bashan and Kurihara, either individually or as a whole, fail to disclose, teach or suggest all the components of claims 13-37. As a result, Bashan and Kurihara fail to anticipate Applicant's invention or render it obvious. The claims are considered allowable for the reasons discussed above, as well as for the additional features they recite.

Because Applicant submits that the Examiner's basis for making the rejection of claims 13-37 is both improper and unreasonable, withdrawal of this rejection is respectfully requested.

In view of the foregoing, it is submitted that the rejection of claims 13-37 is improper and should not be sustained. Therefore, a reversal of the rejection of August 5, 2003 as to claims 13-37 is respectfully requested.

Respectfully submitted,

DATE: October 2 , 2003

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IX. APPENDIX

Claims on Appeal

13. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

14. The portable electronic apparatus according to claim 13, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

15. The portable electronic apparatus according to claim 13, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

16. The portable electronic apparatus according to claim 13, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

17. The portable electronic apparatus according to claim 16, wherein said received signal is a modulated signal.

18. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said IC card by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

19. The IC card according to claim 18, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

20. The IC card according to claim 18, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

21. The IC card according to claim 18, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

22. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said reader/writer by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.

23. The reader/writer according to claim 22, wherein the phase of said clock signal is compared to the phase of said received signal,

said clock signal, when out of phase with said received signal, is brought into phase with said received signal.

24. The reader/writer according to claim 22, wherein said decoder includes a storage medium,

said plurality of logic levels being used to address a storage medium location within said storage medium,

said received data being stored at said storage medium location.

25. The reader/writer according to claim 22, wherein said received signal is wirelessly transmitted to said portable electronic apparatus.

26. A portable electronic apparatus comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said portable electronic apparatus by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

27. The portable electronic apparatus according to claim 26, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

28. The portable electronic apparatus according to claim 26, wherein said first direction is an increasing direction and said

direction opposite to said first direction is a decreasing direction.

29. The portable electronic apparatus according to claim 26, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

30. An IC card for receiving data transmitted by a reader/writer and for outputting data from an internal memory in return, said IC card comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said IC card by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said

first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

31. The IC card according to claim 30, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

32. The IC card according to claim 30, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

33. An IC card according to claim 30, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.

34. A reader/writer for receiving data transmitted by an IC card, said reader/writer comprising:

a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal,

received data being the information transmitted to said reader/writer by way of said received signal; and

a correlation value detection circuit, said correlation value detection circuit comparing the phase of said clock signal to the phase of said received signal to generate a correlation value signal,

said correlation value signal trending in a first direction when said clock signal is in phase with said received signal and trending in a direction opposite to said first direction when said clock signal is out of phase with said received signal;

a determination circuit, said determination circuit using said correlation value signal to generate said received data.

35. The reader/writer according to claim 34, wherein a value of said correlation value signal establishes the logic level of said received data, said logic level being one of a "0" logic level and a "1" logic level.

36. The reader/writer according to claim 34, wherein said first direction is an increasing direction and said direction opposite to said first direction is a decreasing direction.

37. The reader/writer according to claim 34, wherein said correlation value signal is bounded by a maximum amount and a minimum amount, said minimum amount being less than said maximum amount.